AMENDMENTS TO THE CLAIMS

1. (Currently amended) A resistance variable memory element comprising:

a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising:

at least one chalcogenide glass layer,

at least one metal-containing layer,

at least one silver layer provided adjacent to said metal-containing layer, and

at least one other glass layer,

said at least one metal-containing layer and said at least one silver layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer.

2. (Original) The memory element of claim 1 wherein said at least one chalcogenide glass layer comprises a plurality of chalcogenide glass layers.

3. (Original) The memory element of claim 1 wherein said at least one other glass layer comprises a plurality of glass layers.

4. (Original) The memory element of claim 1 wherein said at least one metal-containing layer comprises a silver-chalcogenide.

5. (Original) The memory element of claim 1 wherein said at least one metal-containing layer comprises silver-selenide.

6. (Original) The memory element of claim 1 wherein said at least one metal-containing layer comprises silver-sulfide.

7. (Original) The memory element of claim 1 wherein said at least one metal-containing layer comprises silver-oxide.

8. (Original) The memory element of claim 1 wherein said at least one metal-containing layer comprises silver-telluride.

9. (Original) The memory element of claim 4 wherein said at least one chalcogenide glass layer comprises a material having a stoichiometric formula of Ge_xSe_{100-x}, wherein $20 \alpha x \alpha 43$.

10. (Original) The memory element of claim 9 wherein said material has the formula of about $Ge_{40}Se_{60}$.

11. (Original) The memory element of claim 4 wherein said at least one other glass layer comprises a second chalcogenide glass layer.

12. (Original) The memory element of claim 4 wherein said at least one other glass layer comprises an SiSe composition.

13. (Original) The memory element of claim 4 wherein said at least one other glass layer comprises an AsSe composition.

14. (Original) The memory element of claim 4 wherein said at least one other glass layer comprises a GeS composition.

15. (Original) The memory element of claim 4 wherein said at least one other glass layer comprises a combination of germanium, silver, and selenium.

16. (Original) The memory element of claim 1 wherein said at least one other glass layer has a thickness between about 100 Å and about 1000 Å.

17. (Original) The memory element of claim 1 wherein said at least one other glass layer has a thickness of about 150 Å.

18. (Original) The memory element of claim 1 wherein said at least one chalcogenide glass layer has a thickness between about 100 Å and about 1000 Å.

19. (Original) The memory element of claim 1 wherein said at least one chalcogenide glass layer has a thickness of about 150 Å.

20. (Original) The memory element of claim 1 wherein said at least one metal-containing layer has a first thickness and said at least one chalcogenide glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

21. (Original) The memory element of claim 1 wherein said at least one metal-containing layer has a first thickness and said at least one chalcogenide

glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

22. (Original) The memory element of claim 1 wherein said at least one metal-containing layer comprises a plurality of stacked metal-containing layers.

23. (Original) The memory element of claim 1 wherein said at least one other glass layer comprises at least one second chalcogenide glass layer.

24. (Original) The memory element of claim 23 further comprising at least one second metal-containing layer in contact with said at least one second chalcogenide glass layer, a second silver layer in contact with said second metal-containing layer, and at least one third chalcogenide glass layer in contact with said second silver layer.

25. (Original) The memory element of claim 1 wherein one or more of said at least one chalcogenide glass layers contains a metal dopant.

26. (Original) The memory element of claim 25 wherein said metal dopant comprises silver.

27. (Original) The memory element of claim 1 wherein said at least one metal-containing layer has a first thickness and said at least one other glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

28. (Original) The memory element of claim 1 wherein said at least one metal-containing layer has a first thickness and said at least one other glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

29. (Original) The memory element of claim 1 wherein said at least one metal-containing layer has a thickness equal to or greater than a thickness of each of said at least one chalcogenide glass layer and said at least one other glass layer.

30. (Original) The memory element of claim 1 wherein said silver layer is an evaporated silver layer.

31. (Original) The memory element of claim 1 wherein said silver layer has a thickness of from about 50 Å to about 250 Å.

32. (Original) The memory element of claim 1 further comprising a second silver layer located on a side of said metal-containing layer opposite the side on which said at least one silver layer is located.

33. (Currently amended) A resistance variable memory element comprising:

<u>a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising:</u>

~~a body, said body comprising~~ a first glass layer in contact with at least one silver-chalcogenide layer, and at least one silver layer in contact with said silver-chalcogenide layer, said silver layer being in contact with a second glass layer, wherein at least one of said first and second glass layers is [[a]] formed of a chalcogenide glass material; and

a first electrode and a second electrode in respective contact with said first and second glass layers.

34. (Original) The memory element of claim 33 wherein said at least one silver-chalcogenide layer comprises silver-selenide.

35. (Original) The memory element of claim 33 wherein said at least one silver-chalcogenide layer comprises silver-sulfide.

36. (Original) The memory element of claim 33 wherein said at least one silver-chalcogenide layer comprises silver-oxide.

37. (Original) The memory element of claim 33 wherein said at least one silver-chalcogenide layer comprises silver-telluride.

38. (Original) The memory element of claim 33 wherein said chalcogenide glass material has a stoichiometric formula of Ge_xSe_{100-x}, wherein $20 \alpha x \alpha 43$.

39. (Original) The memory element of claim 33 wherein said material has the formula of about $Ge_{40}Se_{60}$.

40. (Original) The memory element of claim 33 wherein both said first glass layer and said second glass layer comprise a chalcogenide glass material.

41. (Original) The memory element of claim 33 wherein at least one of said first and second glass layers contains a metal dopant.

42. (Currently amended) The memory element of claim [[33]] 41 wherein said metal dopant comprises silver.

43. (Original) The memory element of claim 33 wherein at least another of said first and second glass layers comprises an SiSe composition.

44. (Original) The memory element of claim 33 wherein at least another of said first and second glass layers comprises an AsSe composition.

45. (Original) The memory element of claim 33 wherein at least another of said first and second glass layers comprises a GeS composition.

46. (Original) The memory element of claim 33 wherein at least another of said first and second glass layers comprises a combination of germanium, silver, and selenium.

47. (Original) The memory element of claim 33 wherein said silver-chalcogenide layer has a first thickness, said second glass layer has a second

thickness, and a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

48. (Original) The memory element of claim 33 wherein said silver-chalcogenide layer has a first thickness, said second glass layer has a second thickness, and a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

49. (Original) The memory element of claim 33 wherein said silver-chalcogenide layer has a first thickness and said first glass layer has a second thickness and a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

50. (Currently amended) The memory element of claim 33 wherein said silver-chalcogenide layer has a first thickness, said first ~~second~~ glass layer has a second thickness, and a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

51. (Original) The memory element of claim 33 wherein said silver-chalcogenide layer has a thickness greater than or equal to the thickness of each of said first and second glass layers.

52. (Withdrawn) The memory element of claim 33 wherein at least one of said first and second glass layers contains a metal dopant.

53. (Withdrawn) The memory element of claim 33 wherein said metal dopant comprises silver.

54. (Original) The memory element of claim 33 wherein said silver layer is an evaporated silver layer.

55. (Original) The memory element of claim 33 wherein said silver layer has a thickness of from about 50 Å to about 250 Å.

56. (Original) The memory element of claim 33 further comprising a second silver layer located on a side of said metal-containing layer opposite the side on which said at least one silver layer is located.

57. (Currently amended) A memory element comprising:

a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising:

a first electrode;

a first glass layer comprising Ge_xSe_{100-x}, wherein 20 α x α 43, said first glass layer being in contact with said first electrode;

a first metal-containing layer in contact with said first glass layer;

a first silver layer in contact with said first metal-containing layer;

a second glass layer in contact with said first silver layer; and

a second electrode in contact with said second glass layer.

58. (Original) The memory element of claim 57 wherein x is about 40.

59. (Original) The memory element of claim 57 wherein said first metal-containing layer comprises a silver-chalcogenide.

60. (Original) The memory element of claim 57 wherein said first metal-containing layer comprises silver-selenide.

61. (Original) The memory element of claim 57 wherein said first metal-containing layer comprises silver-sulfide.

62. (Original) The memory element of claim 57 wherein said first metal-containing layer comprises silver-oxide.

63. (Original) The memory element of claim 57 wherein said first metal-containing layer comprises silver-telluride.

64. (Original) The memory element of claim 57 wherein said second glass layer acts as a diffusion control layer to control diffusion of components

from said second electrode through said silver layer, said metal-containing layer, and said first glass layer.

65. (Original) The memory element of claim 57 wherein said second glass layer comprises an SiSe composition.

66. (Original) The memory element of claim 57 wherein said second glass layer comprises an AsSe composition.

67. (Original) The memory element of claim 57 wherein said second glass layer comprises a GeS composition.

68. (Original) The memory element of claim 57 wherein said second glass layer comprises a combination of germanium, silver, and selenium.

69. (Original) The memory element of claim 57 wherein said first metal-containing layer comprises a plurality of metal-containing layers in serial contact with each other.

70. (Original) The memory element of claim 57 wherein at least one of said first glass layer and said second glass layer comprises a plurality of glass layers in serial contact with each other.

71. (Original) The memory element of claim 57 wherein at least one of said first and second glass layers contains a metal dopant.

72. (Original) The memory element of claim 71 wherein said metal dopant comprises silver.

73. (Original) The memory element of claim 57 wherein said first silver layer is an evaporated silver layer.

74. (Original) The memory element of claim 57 wherein said first silver layer has a thickness of from about 50 Å to about 250 Å.

75. (Original) The memory element of claim 57 further comprising a second silver layer located on a side of said metal-containing layer opposite the side on which said first silver layer is located.

76. (Currently amended) A chalcogenide glass stack comprising:

<u>a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising:</u>

a chalcogenide glass layer;

at least one metal-containing layer in contact with said chalcogenide glass layer;

at least one silver layer in contact with said metal-containing layer; and

a diffusion control layer in contact with said silver layer for controlling diffusion of elements into said chalcogenide glass layer.

77. (Original) The chalcogenide glass stack of claim 76 wherein said diffusion control layer is a second glass layer.

78. (Original) The chalcogenide glass stack of claim 76 further comprising a metal-containing electrode in contact with said diffusion control layer and wherein said diffusion control layer slows migration of a metal from said electrode into said chalcogenide glass layer.

79. (Original) The chalcogenide glass stack of claim 76 wherein said at least one metal-containing layer comprises a silver-chalcogenide.

80. (Original) The chalcogenide glass stack of claim 76 wherein said at least one metal-containing layer comprises silver-selenide.

81. (Original) The chalcogenide glass stack of claim 76 wherein said at least one metal-containing layer comprises silver-sulfide.

82. (Original) The chalcogenide glass stack of claim 76 wherein said at least one metal-containing layer comprises silver-oxide.

83. (Original) The chalcogenide glass stack of claim 76 wherein said at least one metal-containing layer comprises silver-telluride.

84. (Original) The chalcogenide glass stack of claim 76 wherein at least one or both of said chalcogenide glass layer and said diffusion control layer contains a metal dopant.

85. (Original) The chalcogenide glass stack of claim 84 wherein said metal dopant comprises silver.

86. (Original) The chalcogenide glass stack of claim 76 wherein said silver layer is an evaporated silver layer.

87. (Original) The chalcogenide glass stack of claim 76 wherein said silver layer has a thickness of from about 50 Å to about 250 Å.

88. (Original) The chalcogenide glass stack of claim 76 further comprising a second silver layer located on a side of said metal-containing layer opposite the side on which said at least one silver layer is located.

89. (Original) A memory element comprising:

a first electrode;

at least one first chalcogenide glass layer in contact with said first electrode;

at least one first metal-containing layer in contact with said at least one first chalcogenide glass layer;

a first silver layer in contact with at said least one first metal-containing layer;

at least one second chalcogenide glass layer in contact with said first silver layer;

at least one second metal-containing layer in contact with said at least one second chalcogenide glass layer;

a second silver layer in contact with at said least one second metal-containing layer;

at least one third chalcogenide glass layer in contact with said second silver layer; and

a second electrode in contact with said at least one third chalcogenide glass layer.

90. (Original) The memory element of claim 89 wherein said metal-containing layers comprise one or more silver-selenide layers.

91. (Original) The memory element of claim 89 wherein one or more of said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

92. (Original) The memory element of claim 89 wherein one or more of said metal-containing layers comprises a plurality of metal-containing layers.

93. (Original) The memory element of claim 89 wherein one or more of said chalcogenide glass layers contains a metal dopant.

94. (Original) The memory element of claim 93 wherein said metal dopant comprises silver.

95. (Original) The memory element of claim 89 wherein each of said first and second silver layers is an evaporated silver layer.

96. (Original) The memory element of claim 89 wherein said first silver layer has a thickness of from about 50 Å to about 250 Å.

97. (Original) The memory element of claim 89 further comprising a third silver layer located on a side of said first metal-containing layer opposite the side on which said first silver layer is located, and a fourth silver layer located on a side of said second metal-containing layer opposite the side on which said second silver layer is located.

98. (Original) A method of forming a resistance variable memory element comprising the steps of:

forming a first electrode;

forming a first chalcogenide glass layer in contact with said first electrode;

forming a first metal-containing layer in contact with said first chalcogenide glass layer;

forming a first silver layer in contact with said first metal-containing layer;

forming a second chalcogenide glass layer in contact with said first silver layer;

forming a second metal-containing layer in contact with said second chalcogenide glass layer;

forming a second silver layer in contact with said second metal-containing layer;

forming a third chalcogenide glass layer in contact with said second silver layer; and

forming a second electrode in contact with said third chalcogenide glass layer.

99. (Original) The method of claim 98 wherein said chalcogenide glass layers comprise a material having the stoichiometric formula Ge_xSe_{100-x}, wherein $20 \alpha x \alpha 43$.

100. (Original) The method of claim 98 wherein said chalcogenide glass layers have a stoichiometry of about $Ge_{40}Se_{60}$.

101. (Original) The method of claim 98 wherein said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

102. (Original) The method of claim 98 wherein said metal-containing layers comprise a plurality of metal-containing layers.

103. (Original) The method of claim 98 wherein one or more of said chalcogenide glass layers contain a metal dopant.

104. (Original) The method of claim 98 wherein one or more of said metal-containing layers comprises silver-selenide.

105. (Original) The method of claim 103 wherein said metal dopant comprises silver.

106. (Original) The method of claim 98 wherein said metal-containing layers have a thickness which is equal to or greater than the thickness of each of said chalcogenide glass layers.

107. (Original) The method of claim 98 wherein each of said metal-containing layers has a first thickness and each of said chalcogenide glass layers has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

108. (Original) The method of claim 107 wherein said thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

109. (Original) The method of claim 98 wherein each of said first and second silver layers is an evaporated silver layer.

110. (Original) The method of claim 98 wherein each of said first and second silver layers has a thickness of from about 50 Å to about 250 Å.

111. (Original) The method of claim 98 further comprising a third silver layer located on a side of said first metal-containing layer opposite the side on which said first silver layer is located, and a fourth silver layer located on a side of said second metal-containing layer opposite the side on which said second silver layer is located.

112. (Currently amended) A method of forming a resistance variable memory element comprising a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said method comprising:

forming a first glass layer;

forming a silver-selenide layer in contact with said first glass layer;

forming at least one silver layer in contact with said silver-selenide layer; and

forming a second glass layer in contact with said silver layer, whereby one of said first and second glass layers is a formed of a chalcogenide glass material.

113. (Original) The method of claim 112 wherein said chalcogenide glass material has a stoichiometric composition of about $Ge_{40}Se_{60}$.

114. (Original) The method of claim 112 wherein at least one of said glass layers contains a metal dopant.

115. (Original) The method of claim 114 wherein said metal dopant comprises silver.

116. (Original) The method of claim 112 wherein both of said first and second glass layers comprises a chalcogenide glass material.

117. (Original) The method of claim 112 further comprising the step of forming alternating layers of said chalcogenide glass material, said silver-selenide layer, and said silver layer.

118. (Currently amended) The method of claim 112 wherein said first or said second glass layer formed of said chalcogenide glass material further contains a metal dopant.

119. (Original) The method of claim 118 wherein said metal dopant comprises silver.

120. (Original) The method of claim 112 wherein another of said first and second glass layers controls diffusion of a metal ion from an electrode through said memory element.

121. (Original) The method of claim 120 wherein said other glass layer comprises an SiSe composition.

122. (Original) The method of claim 120 wherein said other glass layer comprises an AsSe composition.

123. (Original) The method of claim 120 wherein said other glass layer comprises a GeS composition.

124. (Original) The method of claim 120 wherein said other glass layer comprises a combination of germanium, silver, and selenium.

125. (Original) The method of claim 94 wherein said metal-containing layer has a thickness which is equal to or greater than a thickness of each of said first and second glass layers.

126. (Original) The method of claim 112 wherein said metal-containing layer comprises a plurality of silver-selenide layers in serial contact with each other.

127. (Original) The method of claim 112 wherein said silver layer is an evaporated silver layer.

128. (Original) The method of claim 112 wherein said silver layer has a thickness of from about 50 Å to about 250 Å.

129. (Original) The method of claim 112 further comprising a second silver layer located on a side of said silver-selenide layer opposite the side on which said at least one silver layer is located.

130. (Currently amended) A processor-based system, comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit including a resistance variable memory element comprising a plurality of layers configured for retaining stored data as a resistance value and for exhibiting a resistance change in response to an applied programming voltage, said plurality of layers comprising at least one metal-containing layer, at least one silver layer in contact

with said at least one metal-containing layer, at least one chalcogenide glass layer, at least one other glass layer, said metal-containing layer and said silver layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer.

131. (Original) The system of claim 130 wherein said chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein 20 α x α 43.

132. (Original) The system of claim 131 wherein said chalcogenide glass layer stoichiometry is about $Ge_{40}Se_{60}$.

133. (Original) The system of claim 130 wherein at least one of said glass layers contains a metal dopant.

134. (Original) The system of claim 133 wherein said metal dopant comprises silver.

135. (Original) The system of claim 130 wherein said other glass layer comprises a second chalcogenide glass layer.

136. (Original) The system of claim 130 further comprising a second metal-containing layer in contact with said at least one second chalcogenide glass layer, a second silver layer in contact with said second metal-containing layer, and at least one third chalcogenide glass layer in contact with said second silver layer.

137. (Original) The system of claim 130 wherein said chalcogenide glass layer comprises a plurality of stacked chalcogenide glass layers.

138. (Original) The system of claim 130 wherein said metal-containing layer comprises a plurality of stacked metal-containing layers.

139. (Original) The system of claim 130 wherein at least one of said chalcogenide glass layers comprises a metal dopant.

140. (Original) The system of claim 130 wherein said metal-containing layer comprises silver-selenide layer.

141. (Original) The system of claim 130 wherein said other glass layer comprises an SiSe composition.

142. (Original) The system of claim 130 wherein said other glass layer comprises an AsSe composition.

143. (Original) The system of claim 130 wherein said other glass layer comprises a GeS composition.

144. (Original) The system of claim 130 wherein said other glass layer comprises a combination of germanium, silver, and selenium.

145. (Original) The system of claim 130 wherein said other glass layer is a diffusion control layer for slowing migration of a metal ion from an electrode connected thereto.

146. (Currently amended) The system of claim 130 wherein at least one of ~~each of~~ said ~~first and second~~ silver layers is an evaporated silver layer.

147. (Original) The system of claim 130 wherein each of said first and second silver layers has a thickness of from about 50 Å to about 250 Å.

148. (Original) A processor-based system, comprising:

a processor;

a memory circuit connected to said processor, said memory circuit including a first electrode;

at least one first chalcogenide glass layer in contact with said first electrode;

at least one first metal-containing layer in contact with said at least one first chalcogenide glass layer;

at least one first silver layer in contact with said at least one first metal-containing layer;

at least one second chalcogenide glass layer in contact with said at least one first silver layer;

at least one second metal-containing layer in contact with said at least one second chalcogenide glass layer;

at least one second silver layer in contact with said at least one second metal-containing layer;

at least one third chalcogenide glass layer in contact with said at least one second silver layer; and

a second electrode in contact with said at least one third chalcogenide glass layer.

149. (Original) The system of claim 148 wherein said metal-containing layers comprise one or more silver-selenide layers.

150. (Original) The system of claim 148 wherein one or more of said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

151. (Original) The system of claim 148 wherein one or more of said metal-containing layers comprises a plurality of metal-containing layers.

152. (Original) The system of claim 148 wherein one or more of said chalcogenide glass layers contains a metal dopant.

153. (Original) The system of claim 152 wherein said metal dopant comprises silver.

154. (Original) The system of claim 148 wherein each of said at least one first and second silver layers is an evaporated silver layer.

155. (Original) The method of claim 148 wherein each of said at least one first and second silver layers has a thickness of from about 50 Å to about 250 Å.

156. (Original) The method of claim 148 further comprising a third silver layer located on a side of said first metal-containing layer opposite the side on

which said first silver layer is located, and a fourth silver layer located on a side of said second metal-containing layer opposite the side on which said second silver layer is located.

157. (Original) A memory element comprising:

a first electrode;

a second electrode; and

a plurality of chalcogenide glass layers, a plurality of metal-containing layers, and a plurality of silver layers between said first and second electrodes, each of said plurality of metal-containing layers being in contact with at least one of said plurality of silver layers, whereby said plurality of chalcogenide glass layers alternate with said metal-containing layers and said silver layers, with one of said chalcogenide glass layers in contact with said first electrode and another of said chalcogenide glass layers in contact with said second electrode.

158. (Original) The memory element of claim 157 wherein said plurality of metal-containing layers comprises one or more silver-selenide layers.

159. (Original) The memory element of claim 157 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

160. (Original) The memory element of claim 157 wherein one or more of said plurality of metal-containing layers comprises a plurality of metal-containing layers.

161. (Original) The memory element of claim 157 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

162. (Original) The memory element of claim 161 wherein said metal dopant comprises silver.

163. (Original) The memory element of claim 157 wherein each of said plurality of silver layers is an evaporated silver layer.

164. (Original) The memory element of claim 157 wherein each of said plurality of silver layers has a thickness of from about 50 Å to about 250 Å.

165. (Original) A method of forming a resistance variable memory element comprising:

forming a first electrode;

forming a second electrode; and

forming a plurality of chalcogenide glass layers, a plurality of metal-containing layers, and a plurality of silver layers between said first and second electrodes, each of said plurality of metal-containing layers being in contact with at least one of said plurality of silver layers, whereby said plurality of chalcogenide glass layers alternate

with said metal-containing layers and said silver layers, with one of said chalcogenide glass layers in contact with said first electrode and another of said chalcogenide glass layers in contact with said second electrode.

166. (Original) The method of claim 165 wherein said plurality of metal-containing layers comprises one or more silver-selenide layers.

167. (Original) The method of claim 165 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

168. (Original) The method of claim 165 wherein one or more of said plurality of metal-containing layers comprises a plurality of metal-containing layers.

169. (Original) The method of claim 165 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

170. (Original) The method of claim 169 wherein said metal dopant comprises silver.

171. (Original) The method of claim 165 wherein each of said plurality of silver layers is an evaporated silver layer.

172. (Original) The method of claim 165 wherein each of said plurality of silver layers has a thickness of from about 50 Å to about 250 Å.